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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/064,250	04/22/1998	ELIYAHOU HARARI	SNDK.006USM	5711

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EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
02/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/064,250	HARARI ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *63-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *69-73* is/are allowed.

6)☒ Claim(s) *63-68,74 and 75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/22/98* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/17/2007, 12/11/2006, 10/16/2007, 10/11/2005, 06/14/2006, 05/02/2007, 02/13/2006, 01/09/2008.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 63-68 and 74-75 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The independent claims 63 and 74 recite a flash control buffer and an access circuit (or means) and the independent claim 66 recite a data buffer and addressing which are not supported by the specification.

Allowable Subject Matter

3. Claims 69-73 are allowed.

Response to Arguments

4. Applicant's arguments filed 02/13/06 have been fully considered but they are not persuasive. The applicant argues as below

> With respect to the former limitation, it appears that the Office Action identified interface 40 of the present application as "the interface means for exchanging data and addresses with an external system." Because of this identification, the Office Action concluded that FIFOs 519 and 601 "perform the exchange between the microprocessor 21 and the interface 40, not between the flash memory (43) and the interface means (40)," Office Action, paragraph 9, lines 15-17.

However, another component that could be considered as the interface means is controller 31 of Figures 1 B, 6 and 7 (as originally suggested in the Request for Interference of October 19, 1998). **In this case, interface 40 may be considered to be a "flash control buffer means for performing data exchange between the flash memory and the interface means," as it performs data exchange between the flash memory and controller 31**. Similarly, interface 227 of Figure 3A performs data exchange between the flash memory and controller 31.

Alternatively, particular portions of controller 31 may be considered to be the interface means of claim 63. Thus the interface means could include one or more of: microprocessor interface port 505, DMA controller 507, output interface 525 and interface input 603 of Figures 6 and 7. In this case, FIFO 519 of Figure 5 and FIFO 601 of Figure 6 may be considered (individually or jointly) to show "a flash control buffer means for performing data exchange between the flash memory and the interface means." Similarly, receiver 515 (previously misidentified as receiver 313) may be considered to show this feature.

The applicant states "**However, another component that could be considered as the interface means is controller 31 of Figures 1 B, 6 and 7** (as originally suggested in the Request for Interference of October 19, 1998). **In this case, interface 40 may be considered to be a "flash control buffer means for performing data exchange between the flash memory and the interface means," as it performs data exchange between the flash memory and controller 31.**" This argument is found not persuasive since the interface means is different from controller and in this case this controller is a microcomputer system under the control of a microprocessor (see specification page 17, lines 29-31). So, the applicant means the microprocessor (controller 31) is the interface means and the real interface 40 (see Fig.1B) is not an interface but something else such as flash control buffer means which is not ever stated in the specification. The Fig.1B and the specification (page 7, lines 16) teach the interface circuit 40 and the controller 31 are two different means are outside of EEPROM array 33 which including interface circuit 40.

The applicant argues that "Alternatively, **particular portions of controller 31 may be considered to be the interface means** of claim 63. Thus the interface means

could include one or more of: microprocessor interface port 505, DMA controller 507, output interface 525 and interface input 603 of Figures 6 and 7. **In this case, FIFO 519 of Figure 5 and FIFO 601 of Figure 6 may be considered (individually or jointly) to show "a flash control buffer means for performing data exchange between the flash memory and the interface means.**" Similarly, receiver 515 (previously misidentified as receiver 313) may be considered to show this feature." This argument is found not persuasive because this argument is based on a wrong assumption and does not based on the specification as explained above. Therefore, FIFO 519 and 601 can not be considered as a flash control buffer means. The FIFO 519 and 601 are parts of the controller 31 which is not an interface circuit and the controller controls data between system address/data bus 39 and serial data lines 35 and 37. FIFO 519 and 601 in controller 31 do not perform data exchange between the flash memory (43, 45, 47, Fig.1B) and the interface means (40, Fig.1B).

The Office Action stated that cache 705 could not be considered as a flash control buffer means because it is "not for reading and writing together, so it does not perform data exchange (two way transferring of data)," page 5, lines 2-3. However, it is submitted that, to be considered "for performing data exchange," cache 705 does not necessarily have to be involved in every stage of data exchange. Cache 705 is clearly involved in data exchange during writing of data as acknowledged in the Office Action. "Cache 705 is used for holding the data to be write [sic] to flash memory array 33 only (one way transferring data)," page 5, lines 1-2 (emphasis original). However, as one-way transfer is at least part of an exchange, cache 705 may be considered to be • an example of a buffer means for performing data exchange.

Alternatively, cache system 701 of Figure' 8; or a portion thereof, may be considered as a "flash control buffer means for performing data exchange," instead of considering only cache 705. In this case, transfer of data in both directions is performed as indicated by the "Data" line between host interface 703 and flash memory array 33 and described at page 23, lines 31-35. Thus, cache system 701 supports this limitation even if the limitation is given the narrow meaning that the means for performing data exchange must be involved in both reading and writing of data.

Where either cache 705 or cache system 701 (or a portion thereof) is considered as the, buffer means, host interface 703 may be considered as at least a portion of an "interface means for exchanging data and addresses with an external system" of claim 63. Thus, either cache 705

or cache system 701 may be considered to perform "data exchange between the flash memory and the interface means" of claim 63.

Based on incorrect assumption, the applicant considers cache 705 as flash control buffer means. The cache 705 is a part of a cache system 701 which is a part of controller 31 (page 27, lines 4-15) and the controller 31 is different from interface means and can not be an interface means as explained above. Therefore, cache 705 does not perform data exchange between the flash memory (43, 45, 47, Fig.1B) and the interface means (40, Fig.1B) and cache 705 is not a flash control buffer means.

With respect to the "access means for converting" limitation, at least two examples are given in the specification. One example of "access means for converting" of claim 63 is provided by **mapping of defective sectors**. "When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector." Page 23, lines 17-19. The Office Action indicated that this was not considered as "access means for converting" of claim 63 because "such means does not convert any sector address when there is no defective sector," page 7, lines 19-20 (emphasis original). However, the relevance of this statement is not understood. Claim 63 merely requires "access means for converting a sector address," (emphasis added). The Office Action appears to acknowledge that conversion does occur for a defective sector. "The mapping happens only when the defective sector exists,"

The applicant fails to point out which component or which circuit is “access means for converting” as claimed in claims 63 and 74. The applicant only states that “One example of "access means for converting" of claim 63 is provided by **mapping of defective sectors**” and “mapping of defective sectors” is not a circuit or means.

Another example of an "access means for converting" is decoding an address to access the memory. Figure 3A shows decoder 233. "Address information is captured by an address register 231 and is decoded by an address decoder 233," page 10, lines 9-11.

The applicant fails to point out which component or which circuit is “access means for converting” as claimed in claims 63 and 74. The applicant only states that “Another example of an "access means for converting" is decoding an address to access the memory” and “decoding an address” is not a circuit or means.

In short, the specification fails to support *the flash control buffer* for performing data transfer (exchange) between the flash memory and the interface means and *access means for converting* a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vu A. Le/

Primary Examiner, Art Unit 2824

Vu A. Le
Primary Examiner
Art Unit 2824

01/30/2008